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09/753,053	12/28/2000	Ravi Kumar Arimilli	AUS920000670US1	9308

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EXAMINER	
HARKNESS, CHARLES A	

ART UNIT	PAPER NUMBER
2183	5

DATE MAILED: 03/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/753,053	Applicant(s) ARIMILLI ET AL.	
	Examiner Charles A Harkness	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 December 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11, 14-17, and 22-25* is/are rejected.

7)☒ Claim(s) *12,13,18-21 and 26-28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 July 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Papers Submitted

1. It is hereby acknowledged that the following papers have been received and placed of record in the file: Drawings as received on 04/24/01; and Change of Address as received on 07/23/02.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

3. The applicant or their representatives are urged to review the specification and submit corrections for all mistakes of a grammatical, clerical, or typographical nature.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 11 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. Claim 11 recites the limitation "wherein said logic further resets said flag" in line 2 of the claim. There is insufficient antecedent basis for this limitation in the claim. For the purpose of this examination, it will be assumed that claim 11 is dependent on claim 10, which supports the limitations of claim 11.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or

improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

6. Claims 1-2 and 8-9 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 5 of U.S. Patent No. 6,606,702. Although the conflicting claims are not identical, they are not patentably distinct from each other because all of the limitations in claims listed from the instant application are found in the claims of the above patent, and it's not necessary to have an instruction sequencing unit or load/store unit or means responsive to an invalidate to speculatively execute instructions subsequent to a barrier instruction before the barrier instruction is finished executing. As shown in In re Karlson, 153 USPQ 184 (CCPA 1963) elimination of an element or its function generally is not given patentable weight and would have been an obvious improvement. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to delete the unnecessary features or components of the system in the above patent, and thus eliminate its function.

7. Claims 10 and 22 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 6 of U.S. Patent No. 6,606,702. Although the conflicting claims are not identical, they are not patentably distinct from each other because all of the limitations in claims listed from the instant application are found in the claims of the above patent. As shown in In re Karlson, 153 USPQ 184 (CCPA 1963) elimination of an element

or its function generally is not given patentable weight and would have been an obvious. See the double patenting rejection of claims 1-2 and 8-9.

8. Claims 3-5, 11, 15, and 23 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 7 of U.S. Patent No. 6,606,702. Although the conflicting claims are not identical, they are not patentably distinct from each other because all of the limitations in claims listed from the instant application are found in the claims of the above patent. As shown in In re Karlson, 153 USPQ 184 (CCPA 1963) elimination of an element or its function generally is not given patentable weight and would have been an obvious. See the double patenting rejection of claims 1-2 and 8-9.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1-3 and 8-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Morris et al., U.S. Patent Number 6,286,095 (herein referred to as Morris).

10. Referring to claim 1 Morris has taught a method for full speculation of instruction processing in a multiprocessor data processing system (Morris figures 11-12) comprising:

issuing from a processor a barrier operation on a system bus of said data processing system; and

executing operations associated with instructions sequentially following said barrier operation in an instruction sequence prior to completion of said barrier operation (Morris column 4 lines 10-37).

11. Referring to claim 2 Morris has taught the method of Claim 1, wherein said executing step executes said operations, prior to said issuing step (Morris column 6 lines 10-27, figure 11; the execution happens before the issue of the barrier operations).

12. Referring to claim 3 Morris has taught the method of Claim 1, wherein said executing step further comprises:

issuing a load request for data (Morris column 6 lines 10-27, figure 11);

responsive to a return of said data, immediately forwarding said data to a register of said processor (Morris column 6 lines 10-27, figure 11; since execution of the load instruction took place, the data being loaded in would be stored in the register specified by the instruction); and

providing said data to subsequent processes that utilize said data (Morris column 6 lines 10-27, figure 11, column 4 lines 10-37; as long as the ordered load or store instruction was not yet complete, and the instruction that is subsequent is not related, the instruction would use the data that was loaded from the load instruction if required for execution).

13. Referring to claim 8 Morris has taught a multiprocessor computer system comprising:

a plurality of processors interconnected by a system bus, wherein said processors including a first processor that speculatively issues load requests and processes subsequent instructions utilizing data returned by said load request before a completion of a barrier operation that is sequentially before said load requests and subsequent instructions in an instruction sequence (Morris column 4 lines 10-37, column 6 lines 10-27, figure 11; when an ordered store

instruction is being executed, a load request from a load instruction would still be speculatively executed); and

a memory hierarchy connected to said plurality of processors via said system bus that sources said data (Morris column 1 lines 26-42).

14. Referring to claim 9 Morris has taught the multiprocessor computer system of Claim 8, wherein said first processor comprises a load/store unit with logic that controls issuing of load and store instructions before completion of a preceding barrier operation to provide said data to a register of said first processor prior to a return of an acknowledgment for said preceding barrier operations (Morris column 6 lines 10-27, figure 11; since execution of the load instruction took place, the data being loaded in would be stored in the register specified by the instruction).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 4-5 and 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morris in view of Hesson et al., U.S. Patent Number 5,615,350 (herein referred to as Hesson).

16. Referring to claim 4 Morris has not taught the method of claim 3, further comprising setting a flag within said register when said barrier operation has not yet completed, wherein said flag indicates that each instruction executed and each result generated by said subsequent processes and stored within said register is speculative, pending a completion of said barrier

operation. Hesson has taught setting a flag within a register when said barrier operation has not yet completed, wherein said flag indicates that each instruction executed and each result generated by said subsequent processes and stored within said register is speculative (Hesson column 3 line 64-column 4 line 16). The barrier bit indicates that the barrier operation is not yet completed. Therefore, all of the instructions following the barrier operation would be speculatively done before the barrier operation is complete. Hesson does not have a specific barrier operation, but the barrier operation is any operation that would cause a collision. However, one of ordinary skill in the art would recognize how to use a barrier bit in the system of Morris. This allows the system to see that specific instructions, instructions that are dependent on the barrier operation, cannot execute, while other unrelated instructions can continue out-of-order (Hesson column 1 lines 54-67). By doing so, the throughput of the processor is increased. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have a flag to indicate that the barrier operation has not completed to increase the throughput of the processor.

17. Referring to claim 5 Morris and Hesson have taught the method of Claim 4, further comprising:

monitoring for said completion of said barrier operation;

responsive to said completion, resetting said flag and concurrently indicating said register as non speculative (Hesson figure 2B numbers 58 and 59; now that the barrier instruction is completed the bit is reset and execution can continue as normal).

18. Referring to claim 10 Morris has taught the multiprocessor computer system of claim 8, wherein said first processor further comprises:

execution units that processes instructions that utilize said data when said data is placed in said register (Morris would inherently have execution units in each of the processors to execute the instructions).

Morris has not taught wherein said first processor further comprises:

logic, affiliated with said register, that sets a flag within said register when a value resulting from executing said instructions is placed in said register prior to said completion, wherein said flag messages to the execution units that said instruction and said results are speculative, pending a completion of said barrier operation.

19. Referring to claim 11 Morris and Hesson have taught the multiprocessor computer system of claim 10, wherein said logic further resets said flag responsive to said completion (Hesson figure 2B numbers 58 and 59; now that the barrier instruction is completed the bit is reset and execution can continue as normal).

20. Claims 6-7, 14-17, and 22-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morris in view of Hesson in further view of Tran U.S. Patent Number 5,822,575 (herein referred to as Tran).

21. Referring to claim 6 Morris and Hesson have not taught the method of Claim 5, wherein further, when an invalidate is received prior to said completion, said processor discards said data and each of said result from said register. Tran has taught when an invalidate is received prior to said completion, said processor discards said data and each of said result from said register (Tran figure 4 number 84 and 86, column 5 lines 9-38). Tran has taught having a valid bit reset for instructions that have been speculatively executed and then determined to be invalid. The example given is when a branch instruction is predicted and then determined mispredicted. All of

the subsequent instructions that were speculatively executed after the branch instruction are then invalid and must be discarded. By having a bit that can simply be reset to discard invalid data, makes the misprediction recovery process simpler, and quicker, which reduces the time required for execution. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to discard the data when the instructions that were speculatively executed have been determined invalid to insure correct results and reduce the time required for execution.

22. Referring to claim 7 Morris, Hesson, and Tran have taught the method of Claim 6, wherein said operations include load requests and branch instructions, and wherein further said method provides embedded branch speculation within said operations and speculative load request issuing within a branch path (Tran figure 4 number 84 and 86, column 5 lines 9-38).

23. Referring to claims 14 and 22 Morris has taught a processor comprising:

a memory;

at least two processors interconnected to each other and said memory via a system bus, wherein a first processor comprises:

a plurality of execution units including a load/store unit, wherein said load/store unit speculatively executes load requests and offer other execution into speculative execute other instructions before completion of a barrier operation that precedes said load requests and other instructions in an instruction sequence (Morris column 4 lines 10-37, column 6 lines 10-27, figure 11; when an ordered store instruction is being executed, a load request from a load instruction would still be speculatively executed).

Morris has not taught wherein:

a rename register that includes a plurality of entries, wherein each entry has a speculation flag and an associated general purpose register identifier; and

logic for setting said speculation flag to indicate when a value stored in said entry is speculative, pending completion of said barrier operation.

Hesson has taught setting a flag within a register when said barrier operation has not yet completed, wherein said flag indicates that each instruction executed and each result generated by said subsequent processes and stored within said register is speculative (Hesson column 3 line 64-column 4 line 16). Hesson has also taught having the barrier bit in the rename unit (Hesson column 7 lines 35-67). The barrier bit indicates that the barrier operation is not yet completed. Therefore, all of the instructions following the barrier operation would be speculatively done before the barrier operation is complete. Hesson does not have a specific barrier operation, but the barrier operation is any operation that would cause a collision. However, one of ordinary skill in the art would recognize how to use a barrier bit in the system of Morris. This allows the system to see that specific instructions, instructions that are dependent on the barrier operation, cannot execute, while other unrelated instructions can continue out-of-order (Hesson column 1 lines 54-67). By doing so, the throughput of the processor is increased. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have a flag to indicate that the barrier operation has not completed to increase the throughput of the processor. Hesson has not taught having a speculation flag associated with every instruction speculatively executed after the barrier instruction.

Tran has taught when an invalidate is received prior to said completion, said processor discards said data and each of said result from said register (Tran figure 4 number 84 and 86, column 5

lines 9-38). Tran has taught having a valid bit reset for instructions that have been speculatively executed and then determined to be invalid. The example given is when a branch instruction is predicted and then determined mispredicted. All of the subsequent instructions that were speculatively executed after the branch instruction are then invalid and must be discarded. By having a bit that can simply be reset to discard invalid data, makes the misprediction recovery process simpler, and quicker, which reduces the time required for execution. One of ordinary skill in the art would recognize the benefit of combining the valid bits of Tran with the systems of Hesson and Morris to allow for speculative execution after a barrier instruction, and easy recovery after a misprediction, or when the instruction speculatively executed are determined to be invalid. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to discard the data when the instructions that were speculatively executed have been determined invalid to insure correct results and reduce the time required for execution.

24. Referring to claims 15 and 23 Morris has taught the processor of Claim 14, wherein said load/store unit provides data returned by said load requests immediately to an entry of said rename register for utilization within subsequent processes that require said data (Morris column 6 lines 10-27, figure 11, column 4 lines 10-37; as long as the ordered load or store instruction was not yet complete, and the instruction that is subsequent is not related, the instruction would use the data that was loaded from the load instruction if required for execution).

25. Referring to claims 16 and 24 Hesson has taught the processor of Claim 15, wherein said load/store unit messages said execution units and said logic when said barrier operation completes (Hesson figure 2B numbers 58 and 59; now that the barrier instruction is completed the bit is reset and execution can continue as normal).

26. Referring to claims 17 and 25 Tran has taught the processor of Claim 16, wherein, said logic, responsive to a receipt of a message indicating successful completion of said barrier operation, resets each flag associated with a register entry that was speculative with respect to said barrier operation (Tran figure 4 number 84 and 86, column 5 lines 9-38).

Allowable Subject Matter

27. Claims 12-13, 18-21, and 26-28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

28. Morris, Hesson, nor Tran, individually or in combination have taught the limitations of claims 12 or 13.

29. Referring to claim 12 the multiprocessor computer system of claim 11, wherein said first processor further comprises a plurality of execution queues and logic for setting a bit a associated with an entry of said queues to indicate whether an instruction placed in said entry is speculative with respect to said barrier operation.

30. Referring to claim 13 the multiprocessor computer system of claim 11, wherein said first processor further comprises a plurality of execution queues and logic for setting a bit a associated with an entry of said queues to indicate s whether an instruction placed in said entry is speculative with respect to an unresolved branch instruction that precedes said instruction in said instruction sequence.

31. Referring to claims 18 and 26 the processor of Claim 17, further comprising:

a plurality of issue queues associated with said execution units in which instructions to be executed are placed; and

logic for indicating that a particular instruction within one of said issue queues is speculative with respect to the barrier operation.

32. Referring to claims 19 the processor of Claim 17, further comprising:

a plurality of issue queues associated with said execution units in which instructions to be executed are placed; and

logic for indicating that a particular instruction within one of said issue queues is speculative with respect to an unresolved branch instruction that precedes said instruction within said instruction sequence.

33. Referring to claims 20 and 27 the processor of Claim 18, further comprising:

an enhanced internal instruction set architecture that includes a setable bit, which indicates whether an instruction is speculative, wherein said logic sets said setable bit responsive to whether said barrier operation has completed; and

when said barrier operation has completed, said logic resets said bit.

34. Referring to claims 21 and 28 the processor of Claim 18, wherein said issue queues includes a speculation bit associated with each entry location, wherein said speculation bit is set by said logic when said particular instruction is placed in an associated entry location, and reset only when said barrier operation has successfully completed.

Conclusion

35. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR 1.111(c).

Sato, U.S. Patent Number 6,415,380, which has taught the speculative execution of a load instruction by associating the load instruction with a previously executed store instruction.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Charles A Harkness whose telephone number is 703-305-7579. The examiner can normally be reached on 8:00 A.M. – 5:30 P.M. with every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 703-305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-7579.

Charles Allen Harkness

Examiner

Art Unit 2183

March 12, 2004

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
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